000CAT 99T86960

FIG. 1

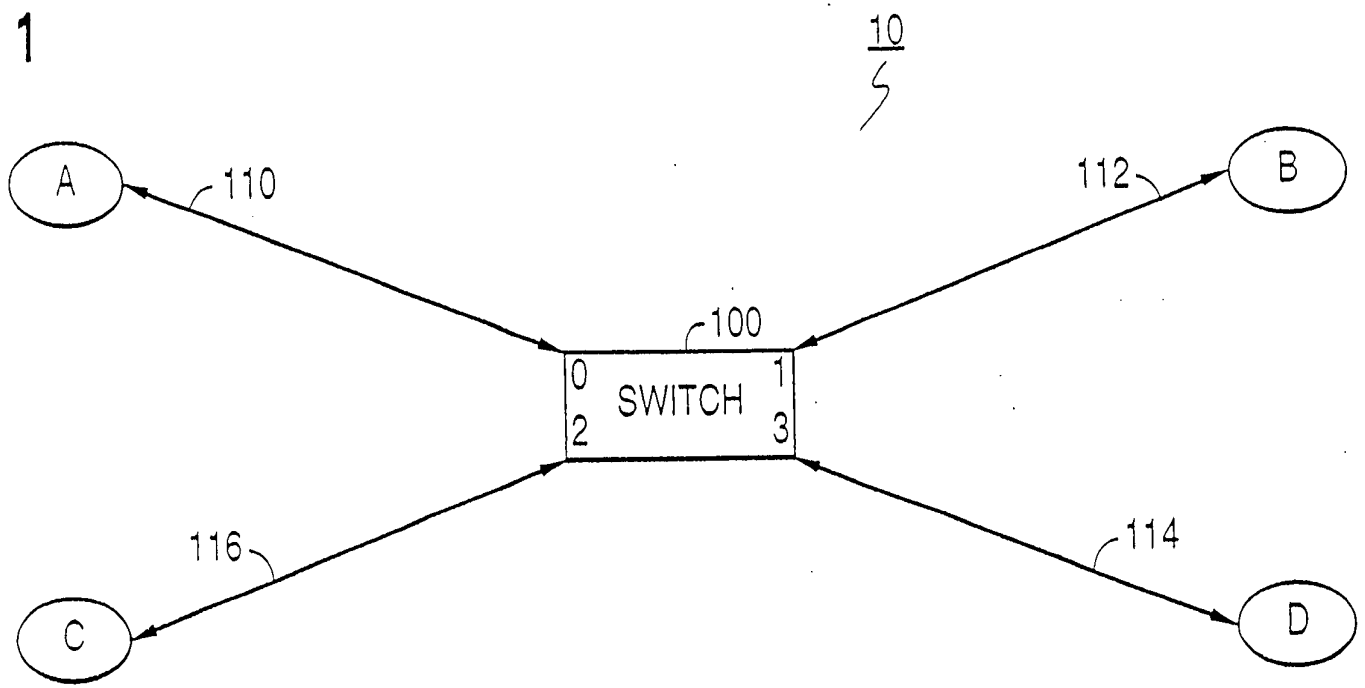
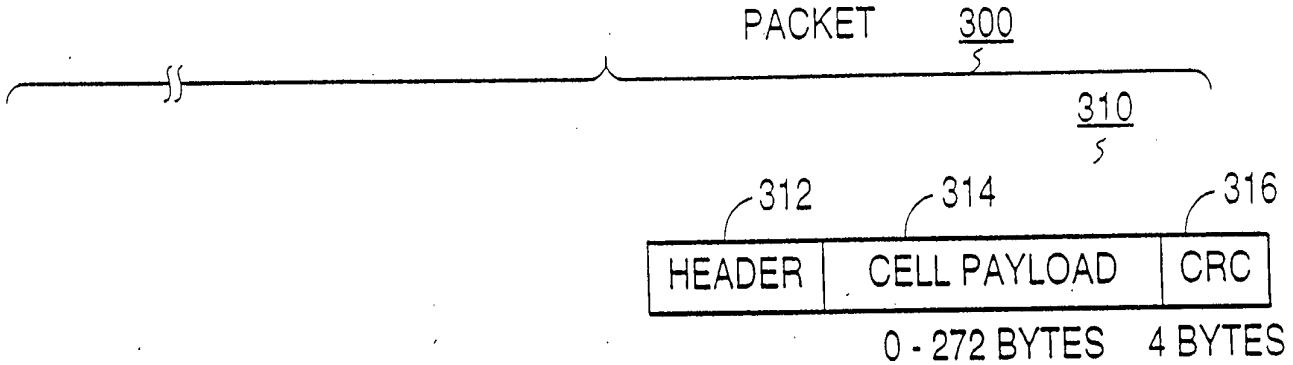


FIG. 3A



000CAT' 98T86960

FIG. 2

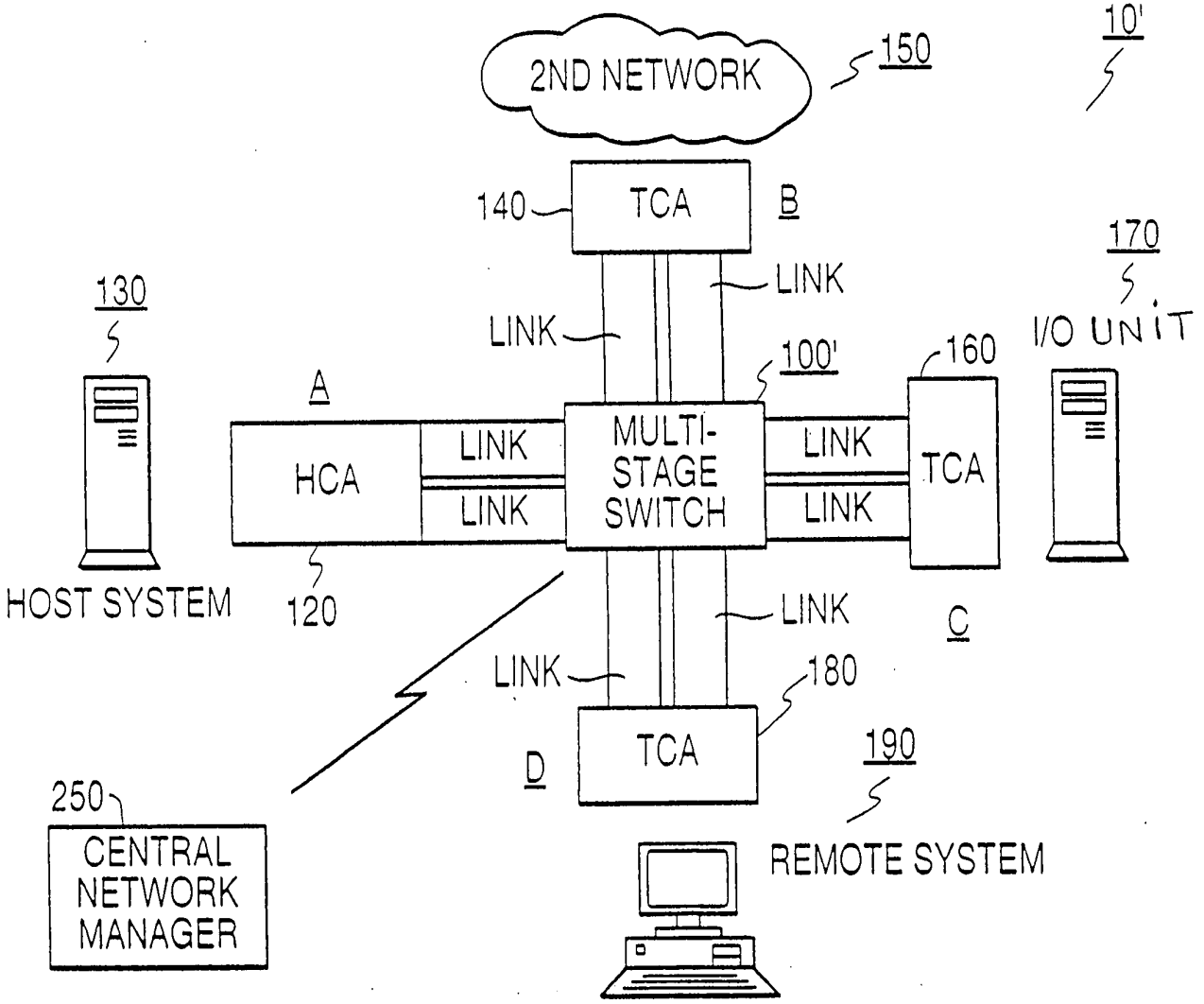
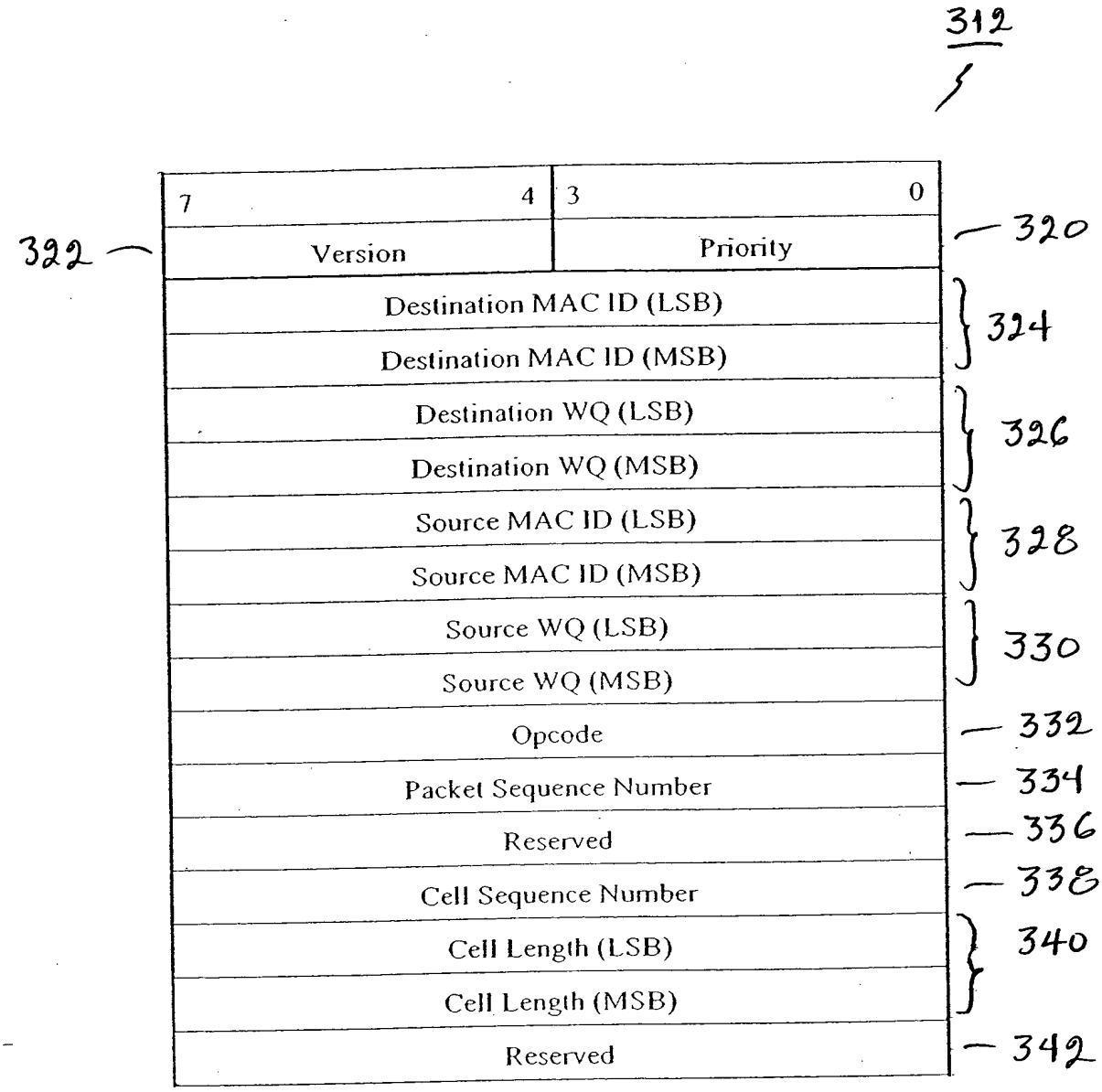


FIG. 3B


312
7
4
3
0
322
Version
Priority
320
Destination MAC ID (LSB)
Destination MAC ID (MSB)
324
Destination WQ (LSB)
Destination WQ (MSB)
326
Source MAC ID (LSB)
Source MAC ID (MSB)
328
Source WQ (LSB)
Source WQ (MSB)
330
Opcode
332
Packet Sequence Number
334
Reserved
336
Cell Sequence Number
338
Cell Length (LSB)
Cell Length (MSB)
340
Reserved
342

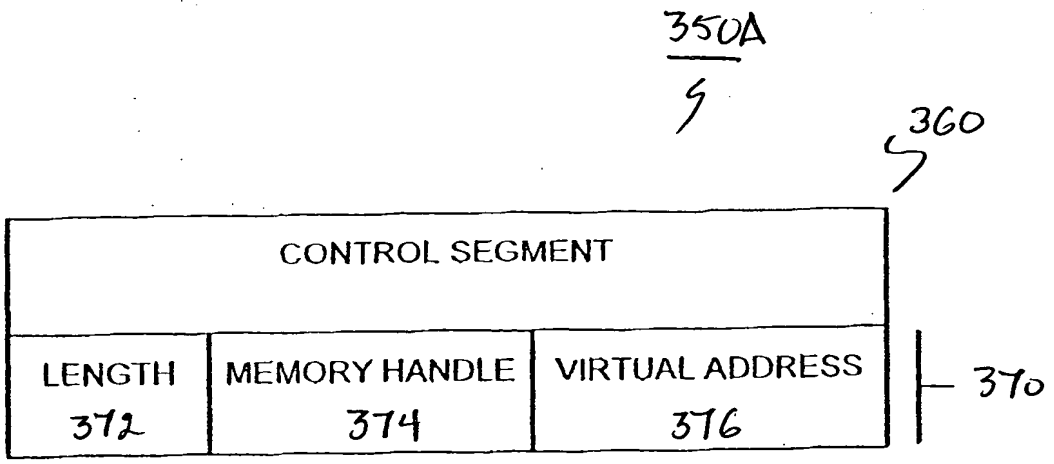

350A
360
CONTROL SEGMENT
LENGTH
372
MEMORY HANDLE
374
VIRTUAL ADDRESS
376
370

FIG. 3C

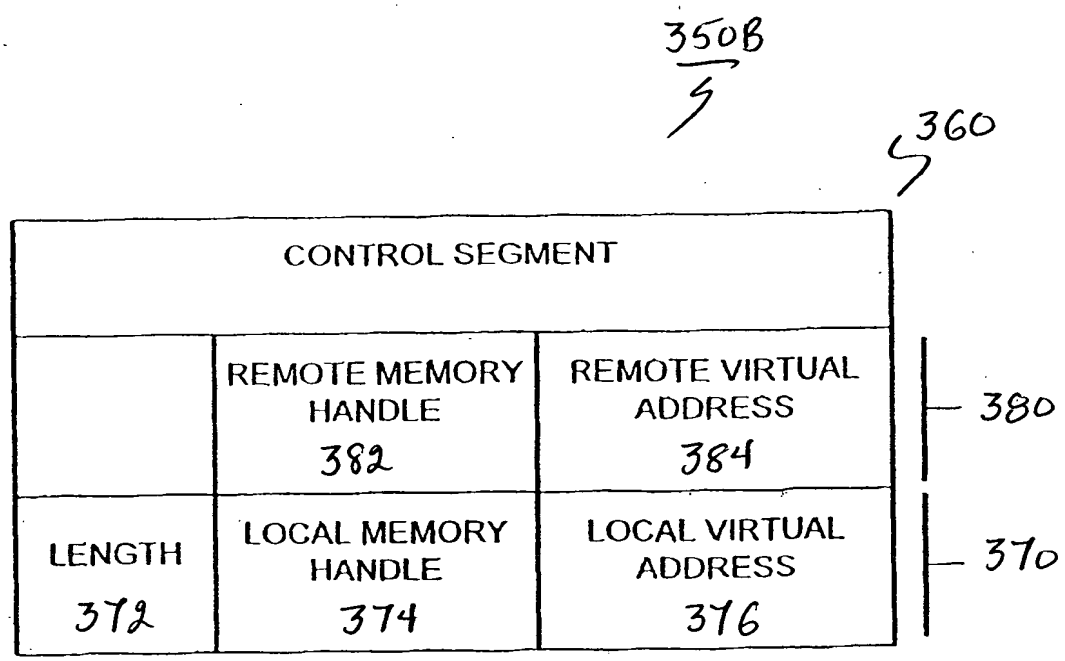

350B
360
CONTROL SEGMENT
REMOTE MEMORY HANDLE
382
REMOTE VIRTUAL ADDRESS
384
380
LENGTH
372
LOCAL MEMORY HANDLE
374
LOCAL VIRTUAL ADDRESS
376
370

FIG. 3D

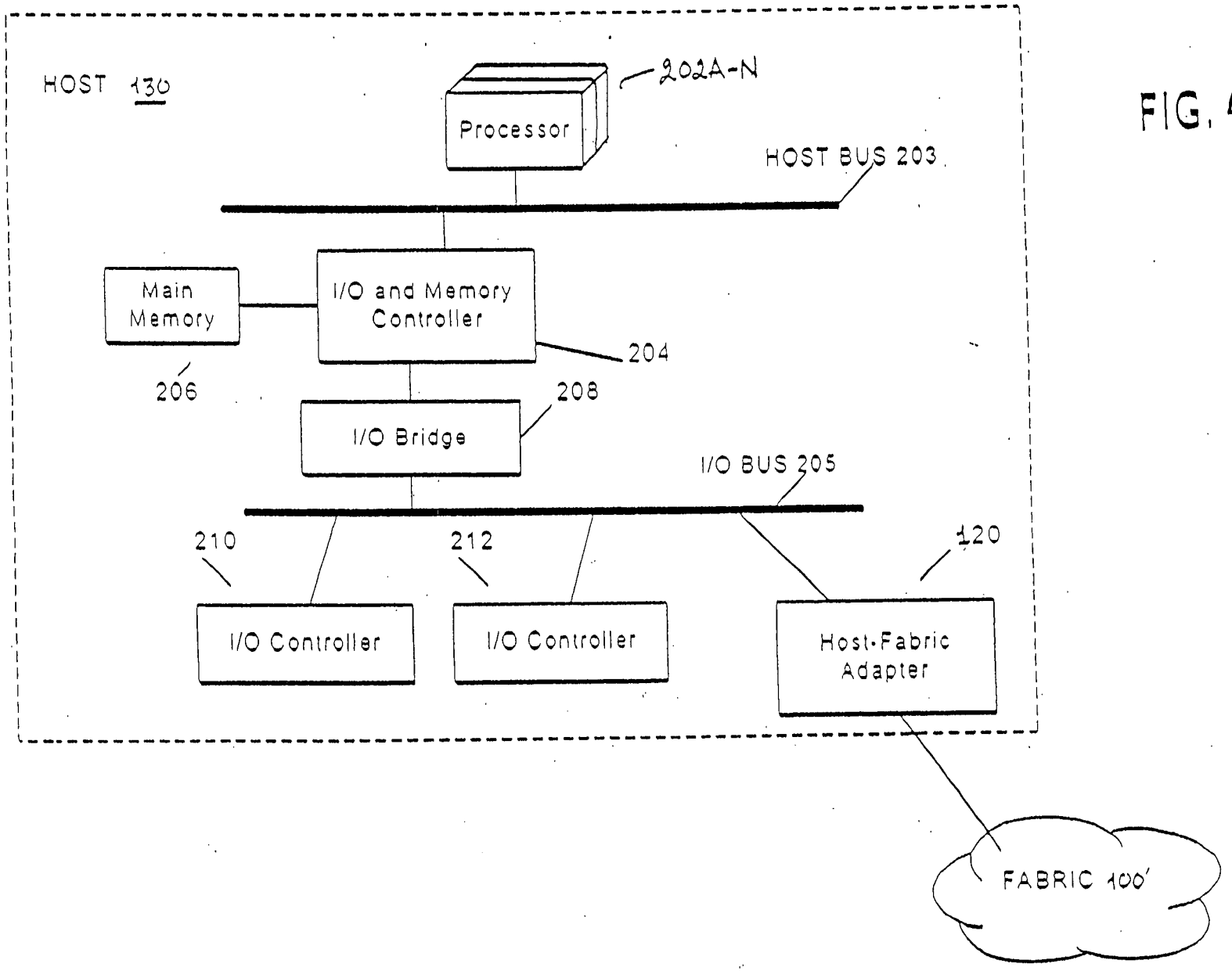

HOST 130
Processor
202A-N
HOST BUS 203
Main Memory
I/O and Memory Controller
204
206
208
I/O Bridge
I/O BUS 205
210
212
120
I/O Controller
I/O Controller
Host-Fabric Adapter
FABRIC 100'

FIG. 4A

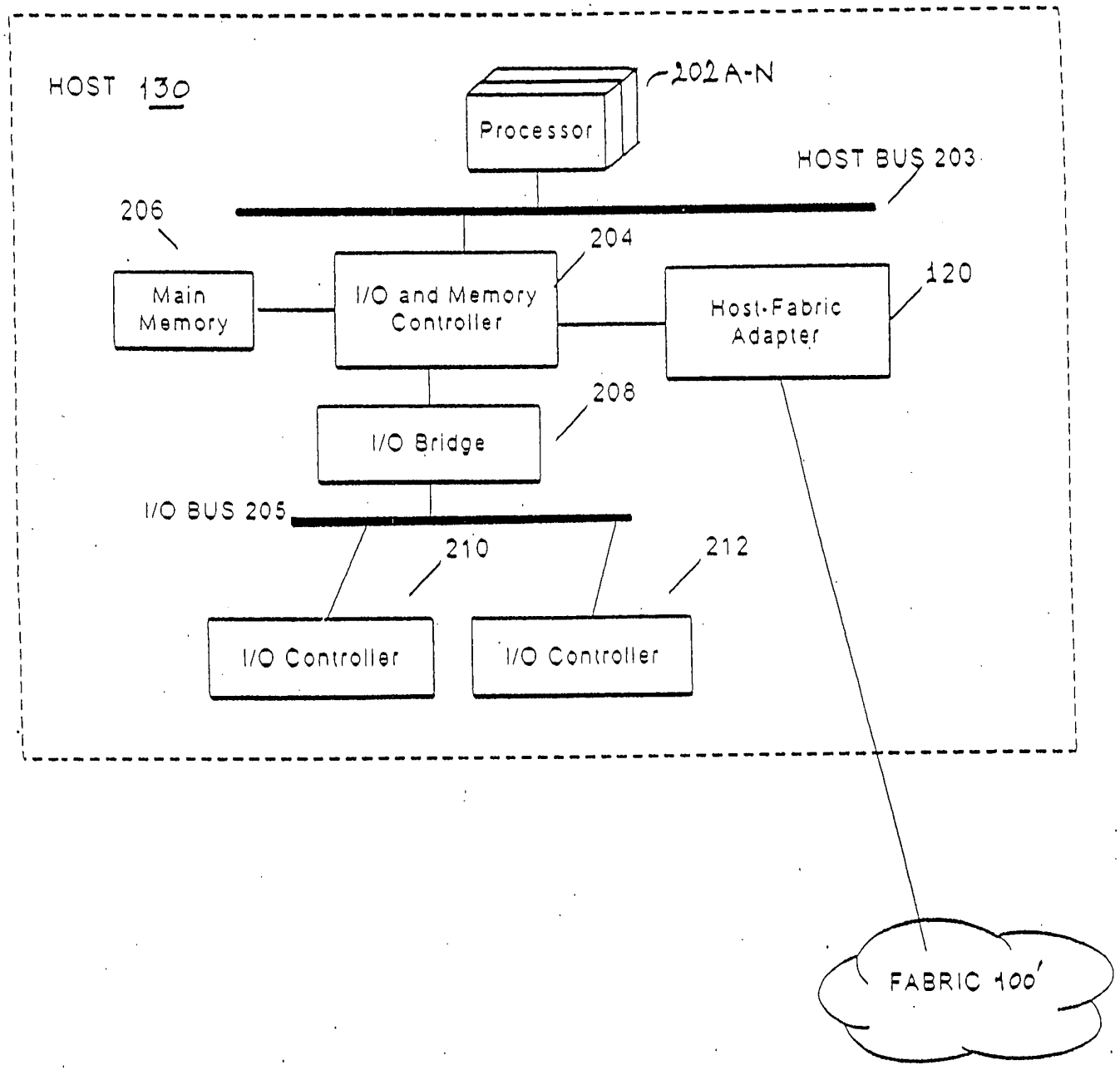
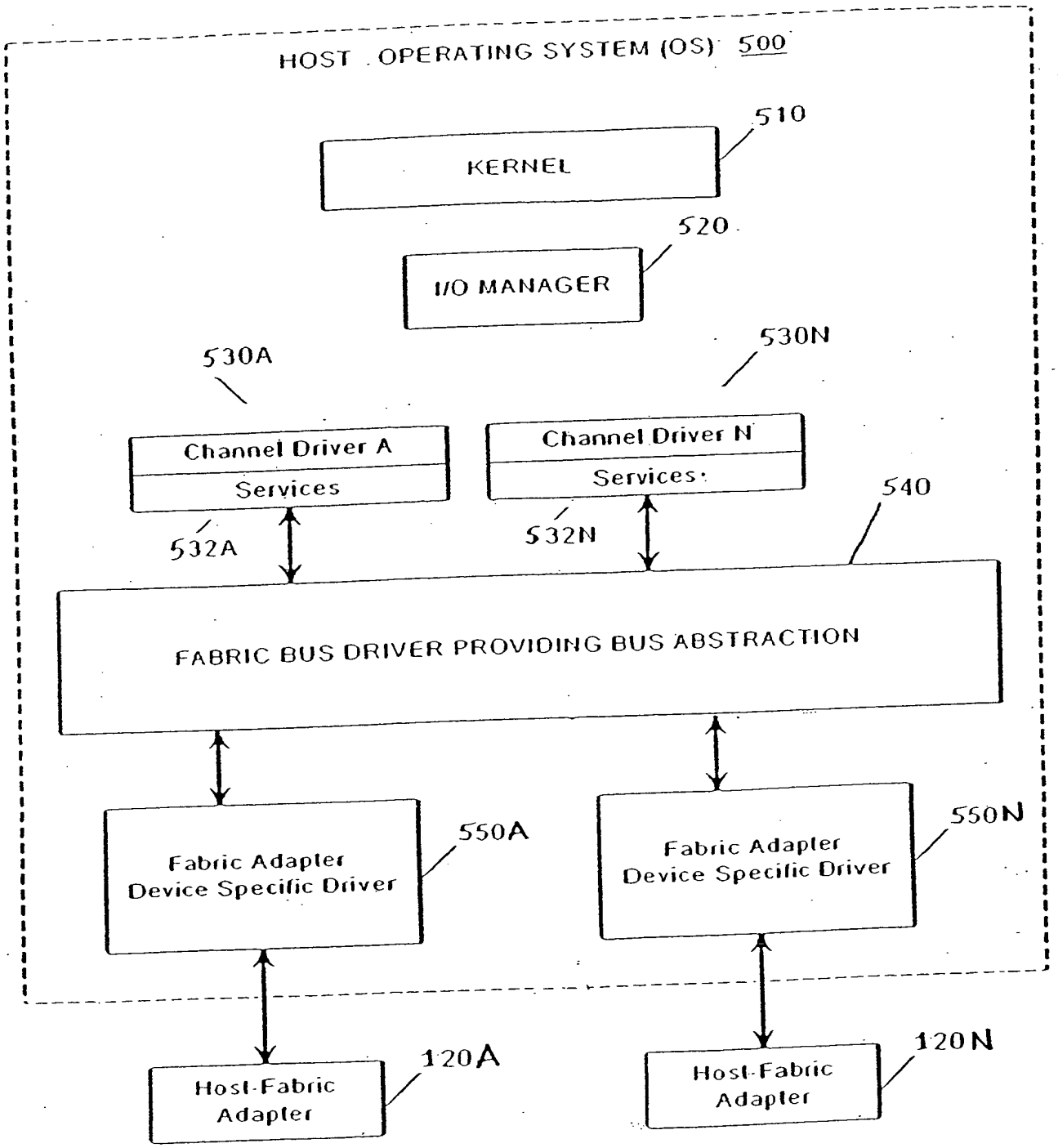

HOST 130
Processor
202A-N
HOST BUS 203
206
204
Main Memory
I/O and Memory Controller
Host-Fabric Adapter
120
208
I/O Bridge
I/O BUS 205
210
212
I/O Controller
I/O Controller
FABRIC 100'

FIG. 4B



EXAMPLE SOFTWARE DRIVER STACKS OF HOST SYSTEM

FIG. 5

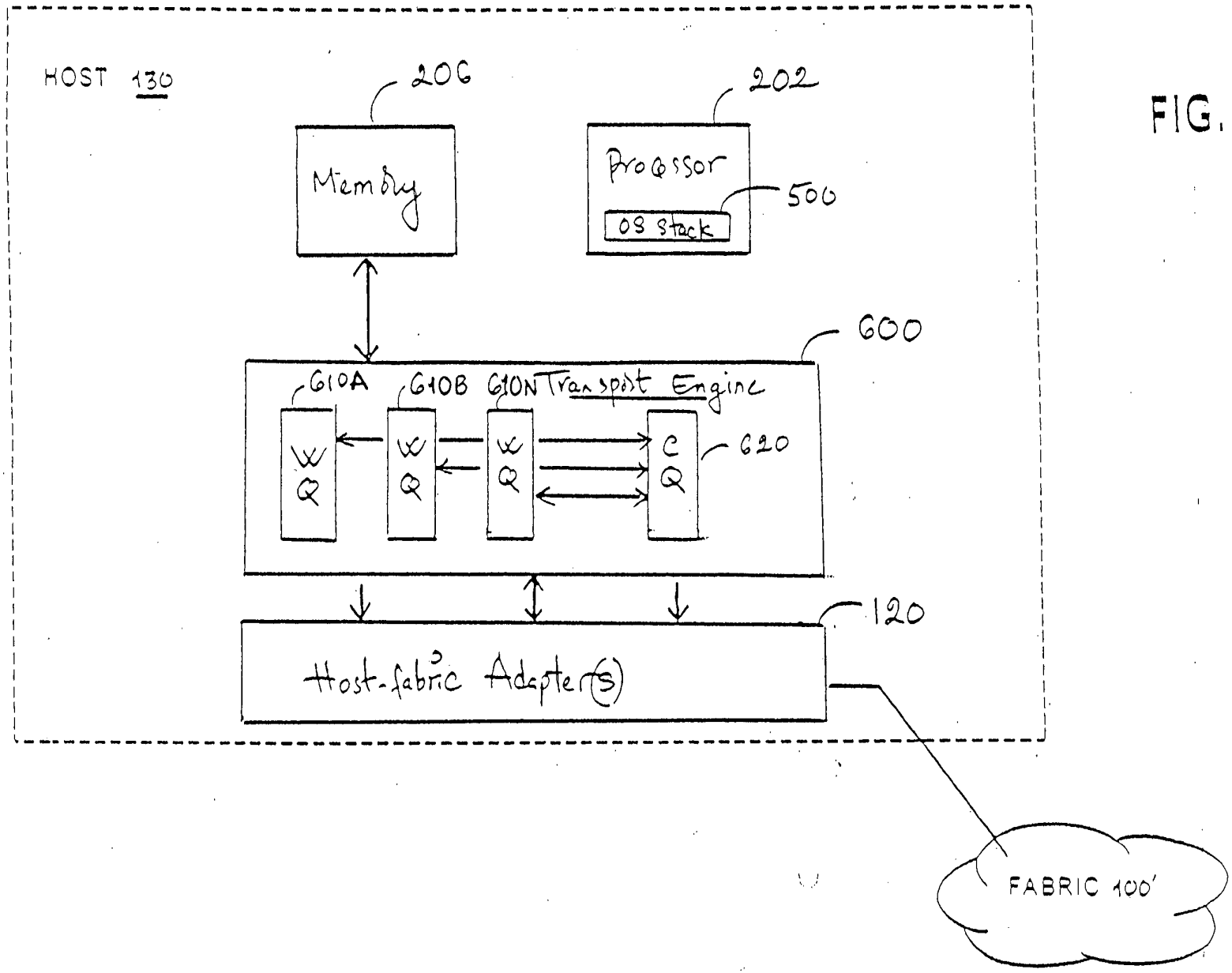

HOST 130
206
Memory
202
Processor
500
OS Stack
600
610A
610B
610N Transport Engine
WQ
WQ
WQ
CQ
620
120
Host-fabric Adapter(s)
FABRIC 100'

FIG. 6

FIG. 7

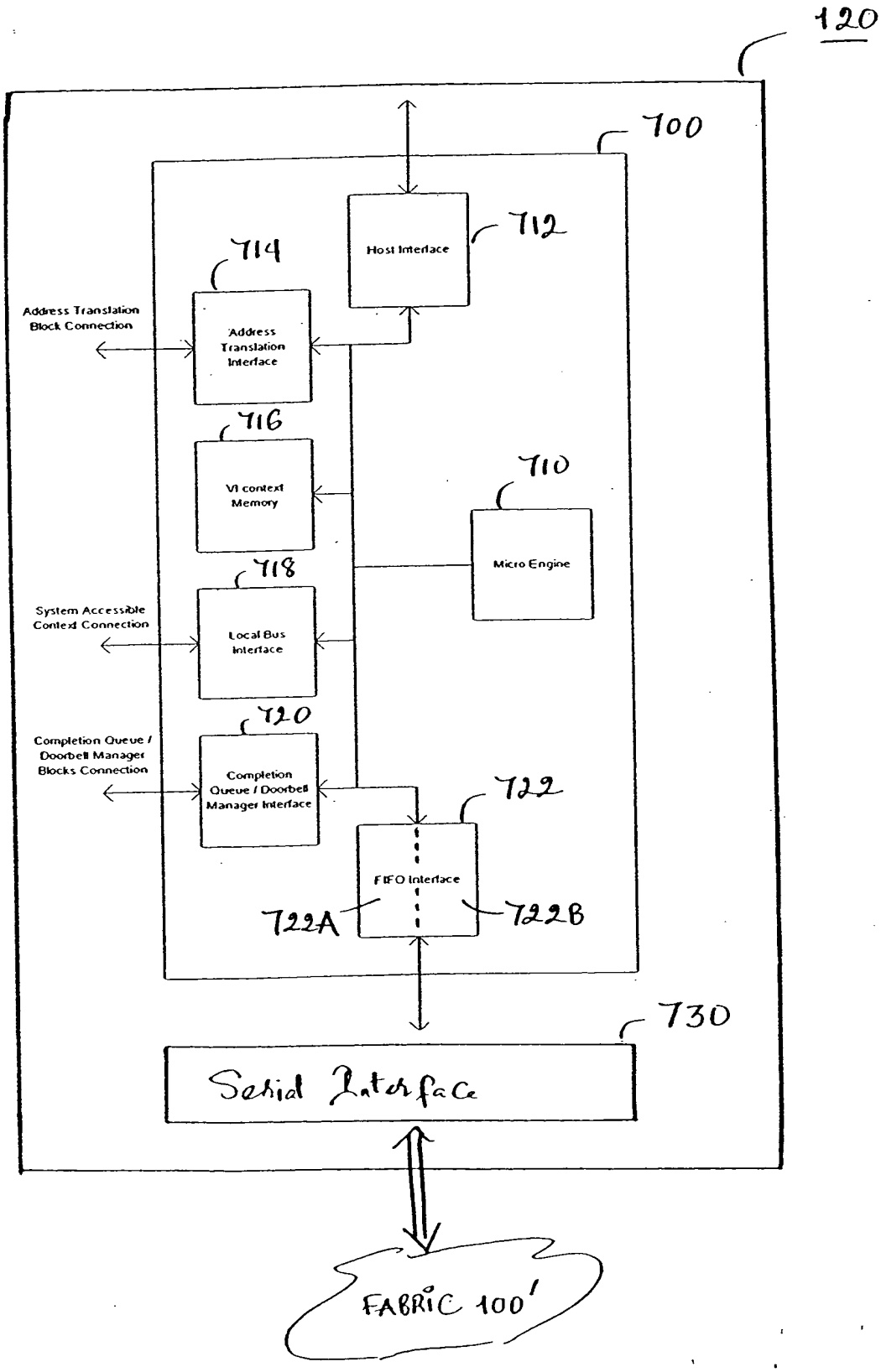

120
700
Host Interface
712
714
Address Translation Block Connection
Address Translation Interface
716
VI context Memory
710
Micro Engine
718
System Accessible Context Connection
Local Bus Interface
720
Completion Queue / Doorbell Manager Blocks Connection
Completion Queue / Doorbell Manager Interface
722
FIFO Interface
722A
722B
730
Serial Interface
FABRIC 100'

FIG. 8

710

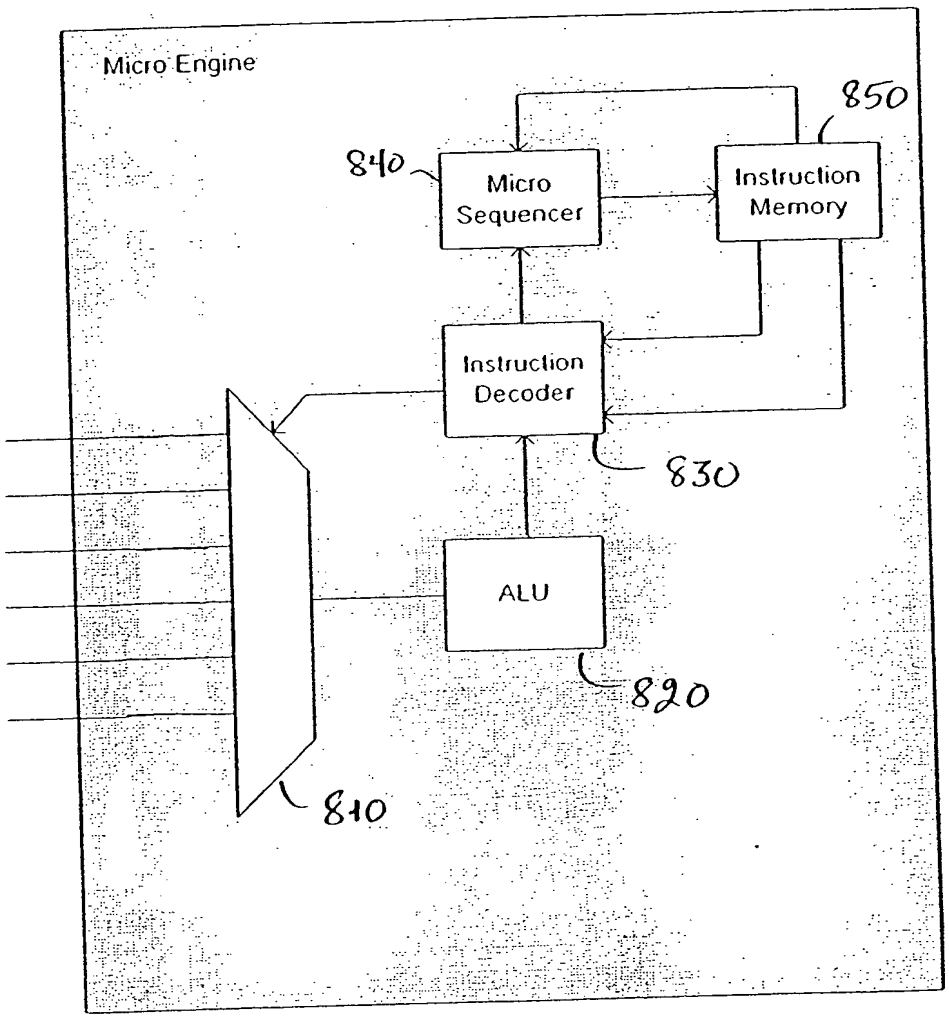

Micro Engine
850
840
Micro Sequencer
Instruction Memory
Instruction Decoder
830
ALU
820
810

FIG. 9

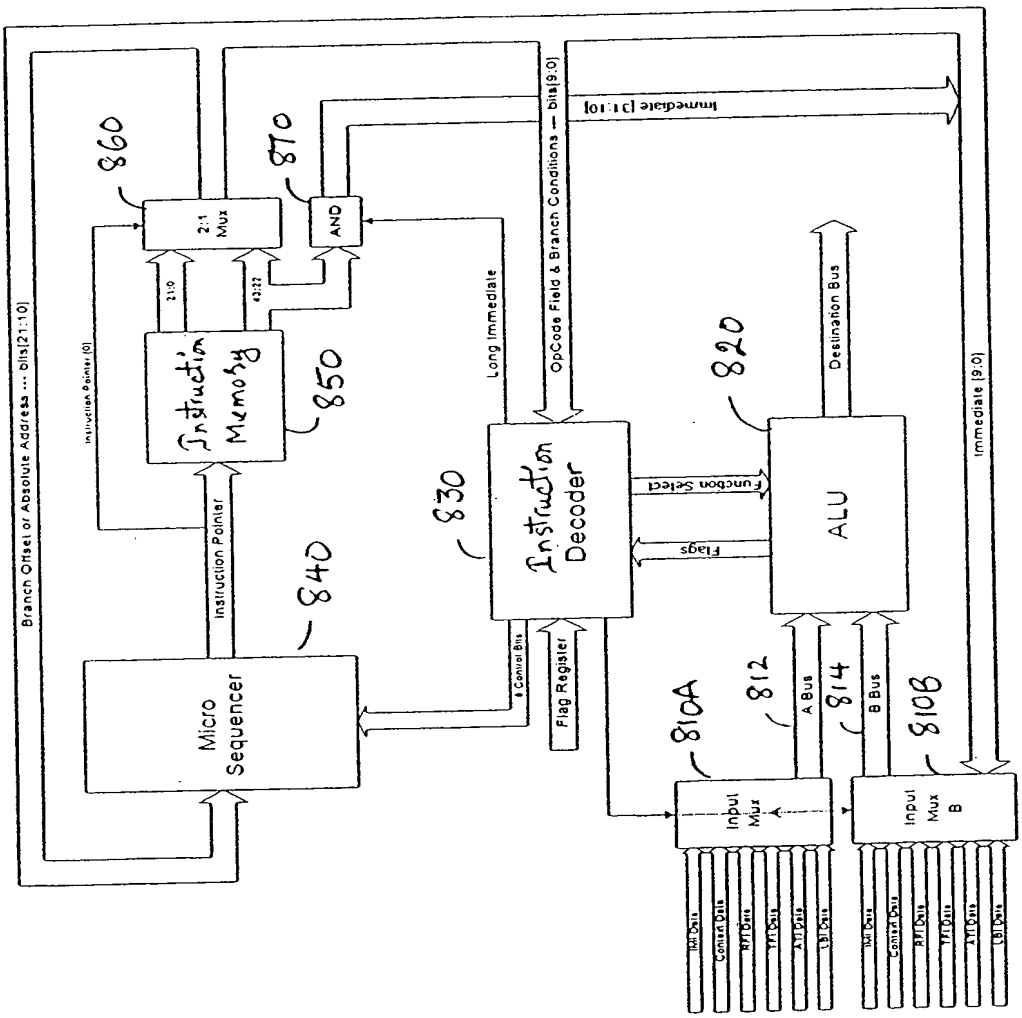

710
860
870
2:1 Mux
AND
Instruction Memory
850
840
Micro Sequencer
Instruction Pointer
Branch Offset or Absolute Address ... bits[21:10]
Instruction Pointer [0]
Long Immediate
OpCode Field & Branch Conditions — bits[9:0]
Immediate [21:10]
Immediate [9:0]
830
Instruction Decoder
Function Select
Flags
820
ALU
Destination Bus
A Control Bits
Flag Register
810A
812
A Bus
814
B Bus
810B
Input Mux
Input Mux B
Ref Data
Control Data
RF Data
YF Data
XF Data
LB Data

FIG. 10

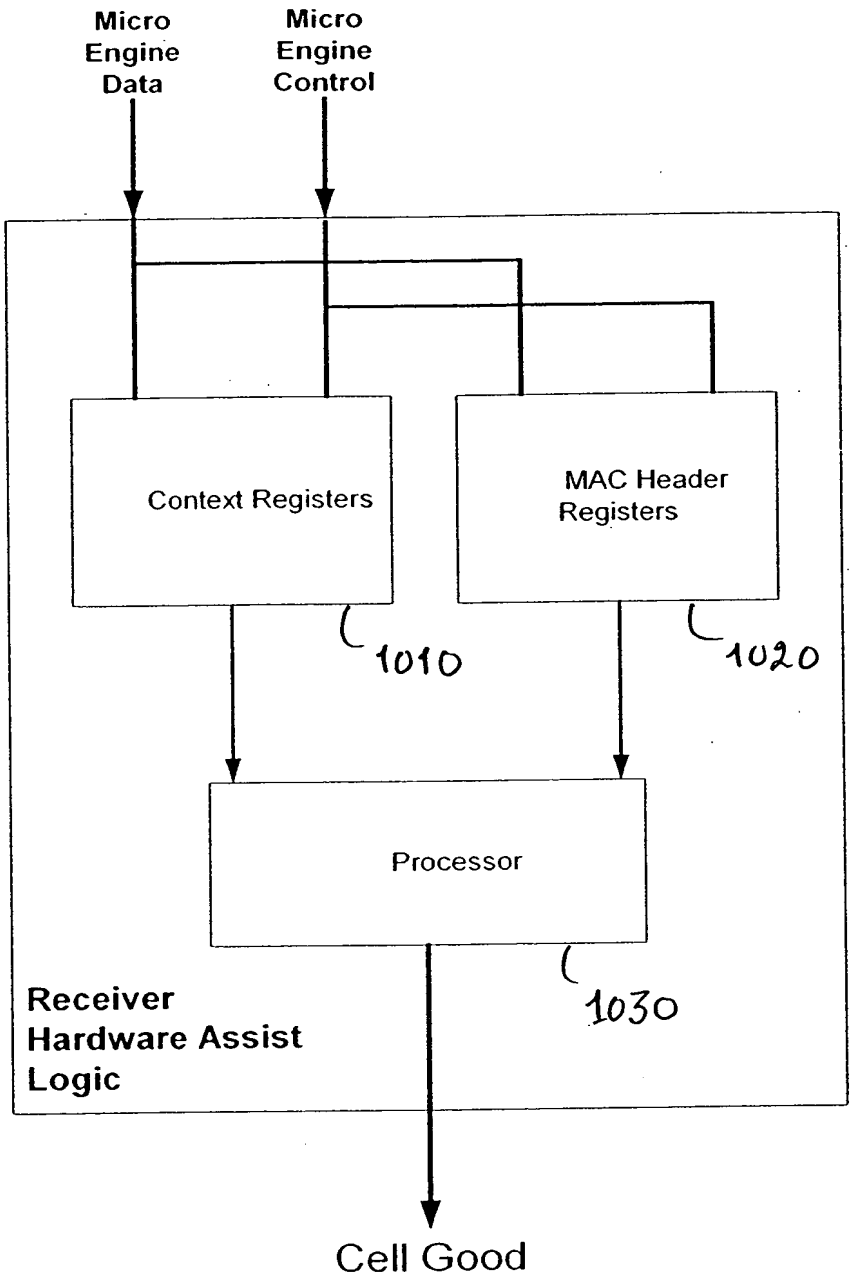

Micro Engine Data
Micro Engine Control
Context Registers
MAC Header Registers
1010
1020
Processor
1030
Receiver Hardware Assist Logic
Cell Good

FIG. 11

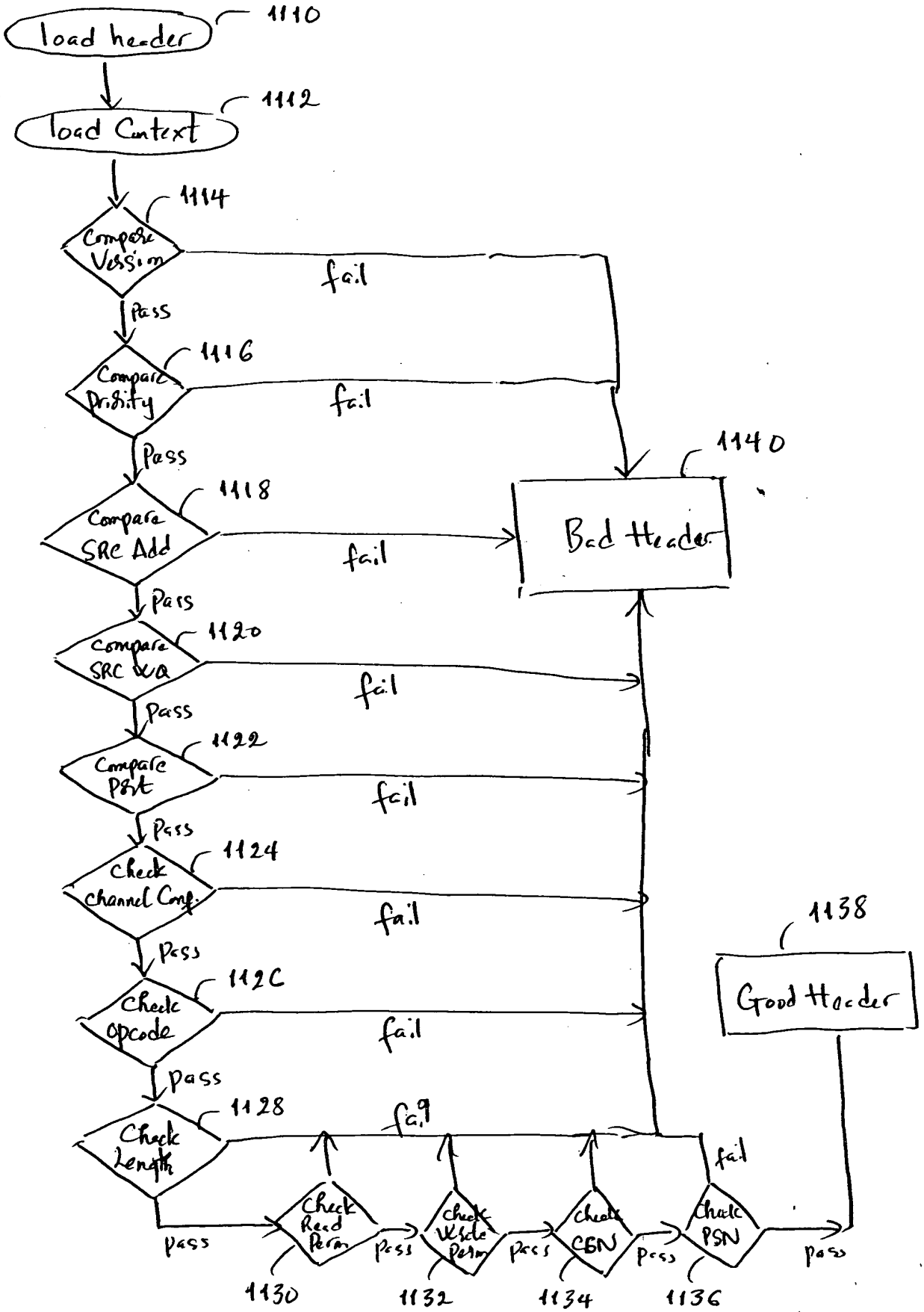

load header
1110
load Context
1112
Compare Version
1114
fail
pass
Compare Priority
1116
fail
pass
Compare SRC Add
1118
fail
Bad Header
1140
pass
Compare SRC VA
1120
fail
pass
Compare PSN
1122
fail
pass
Check channel Conf.
1124
fail
pass
Check opcode
112C
fail
pass
Check Length
1128
fail
pass
Check Read Perm.
1130
pass
Check Write Perm.
1132
pass
Check CSN
1134
pass
Check PSN
1136
fail
pass
Good Header
1138

FIG. 12

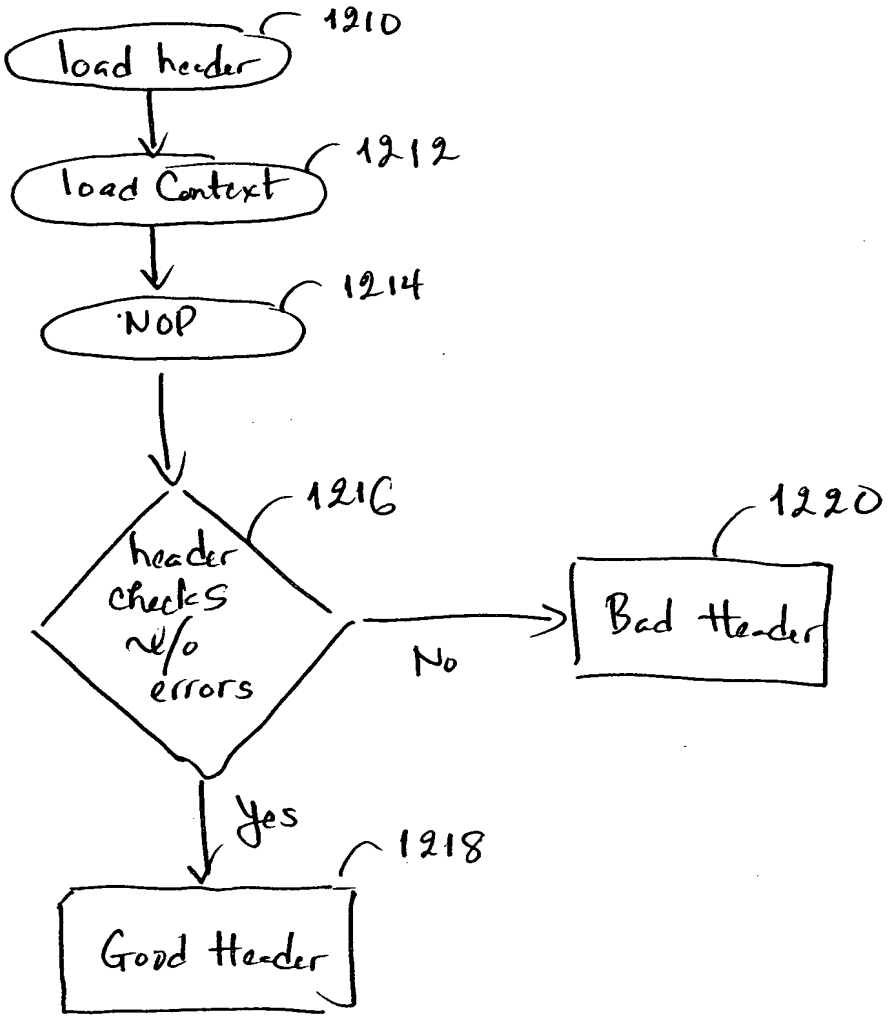

1210
load header
1212
load Context
1214
NOP
1216
header checks w/o errors
No
1220
Bad Header
Yes
1218
Good Header

FIG. 13A

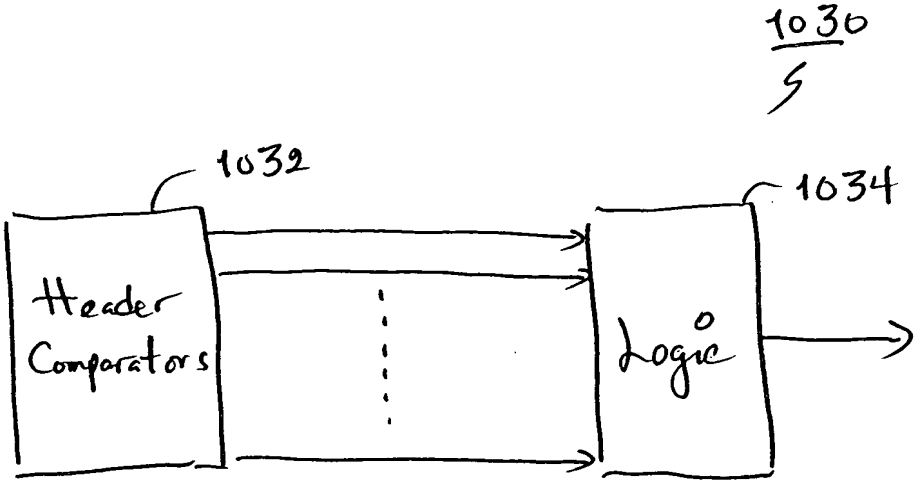


FIG. 13B

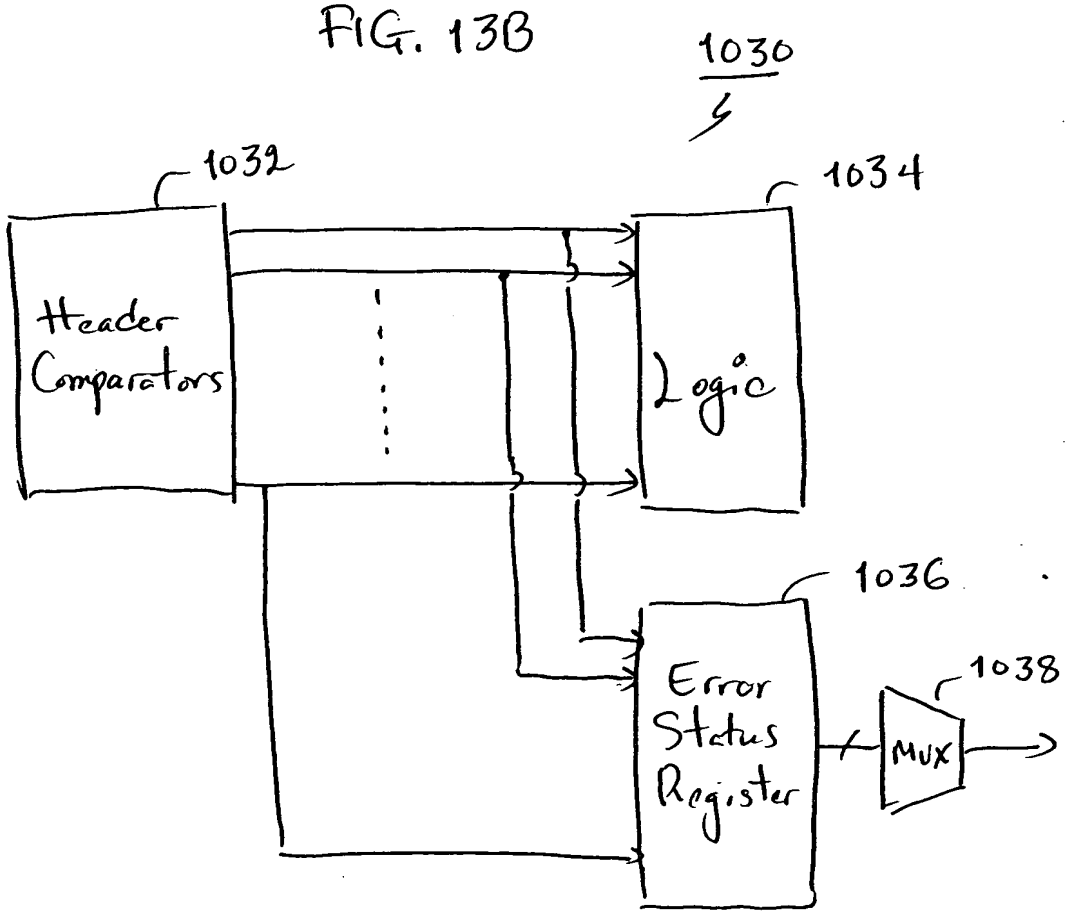


FIG. 14A

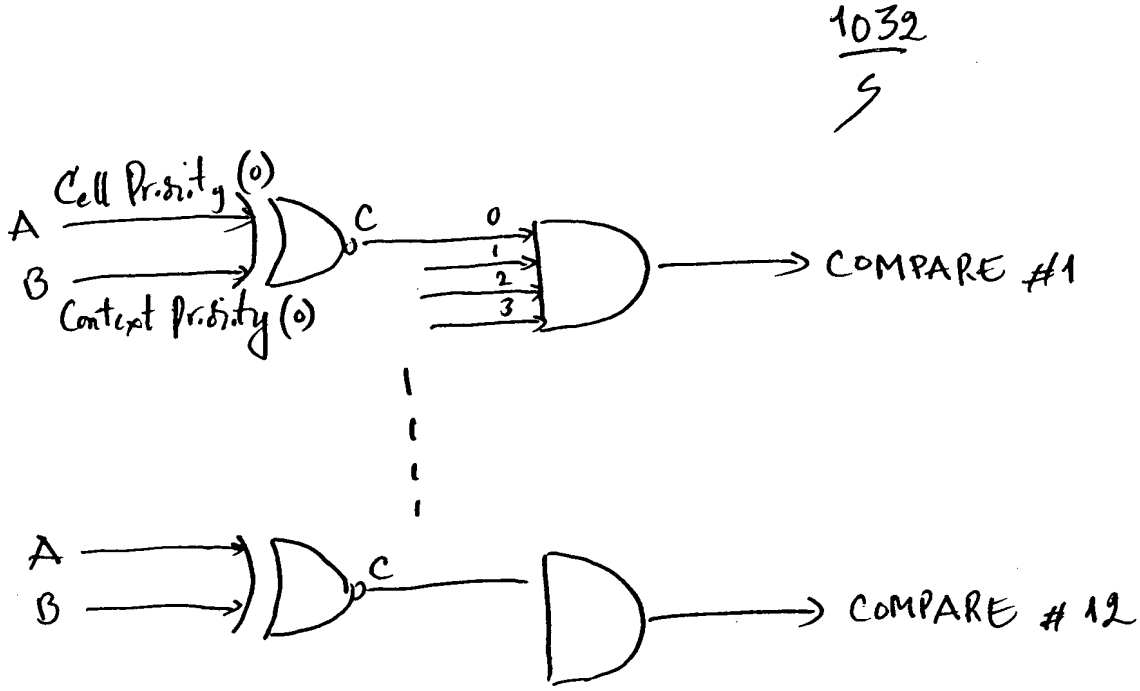


FIG. 14B

1032

XNOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

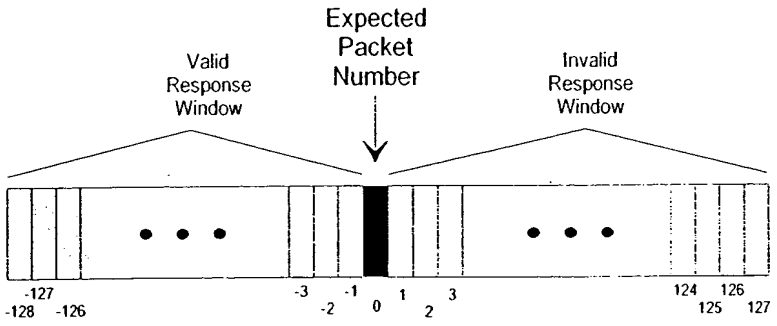


Figure 15 Definition of Earlier and Later Packets

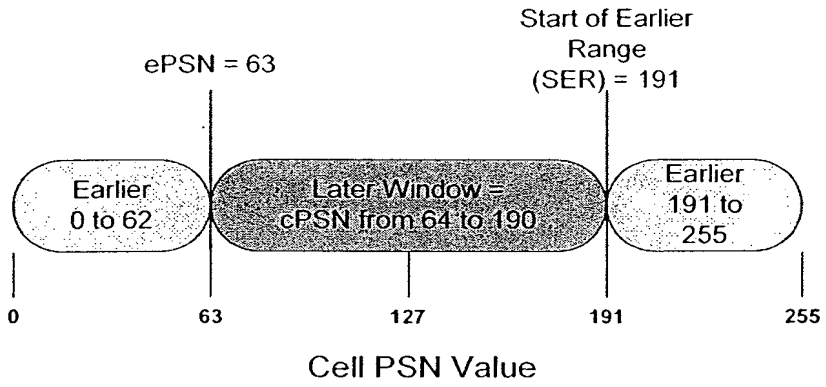


Figure 16 Later Window without Wrap

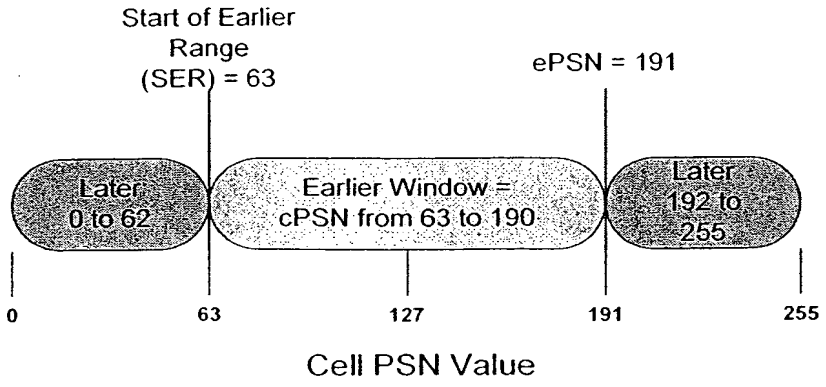


Figure 17 Earlier Window without Wrap

0005075 "9979696"

FIG. 18

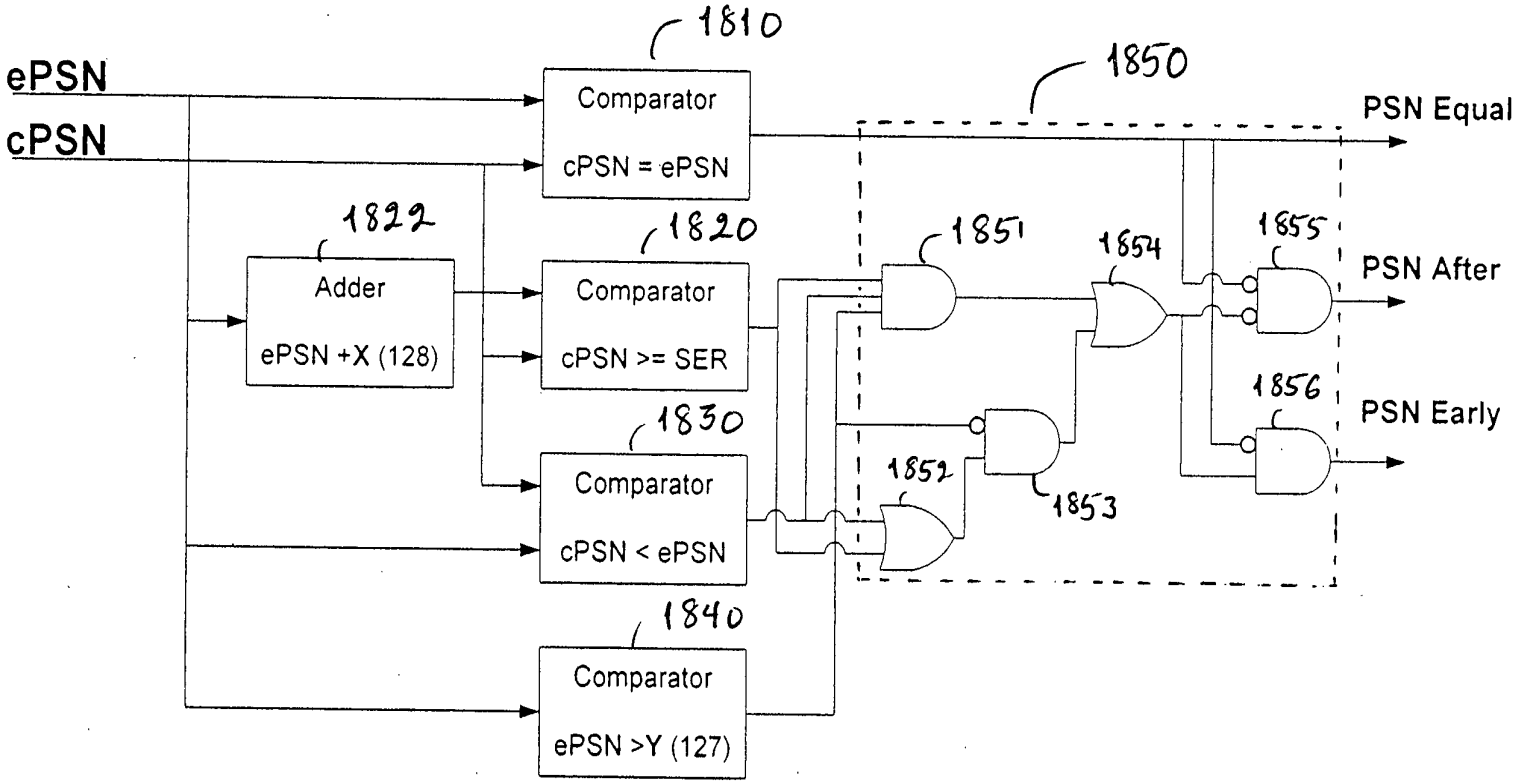


FIG. 19

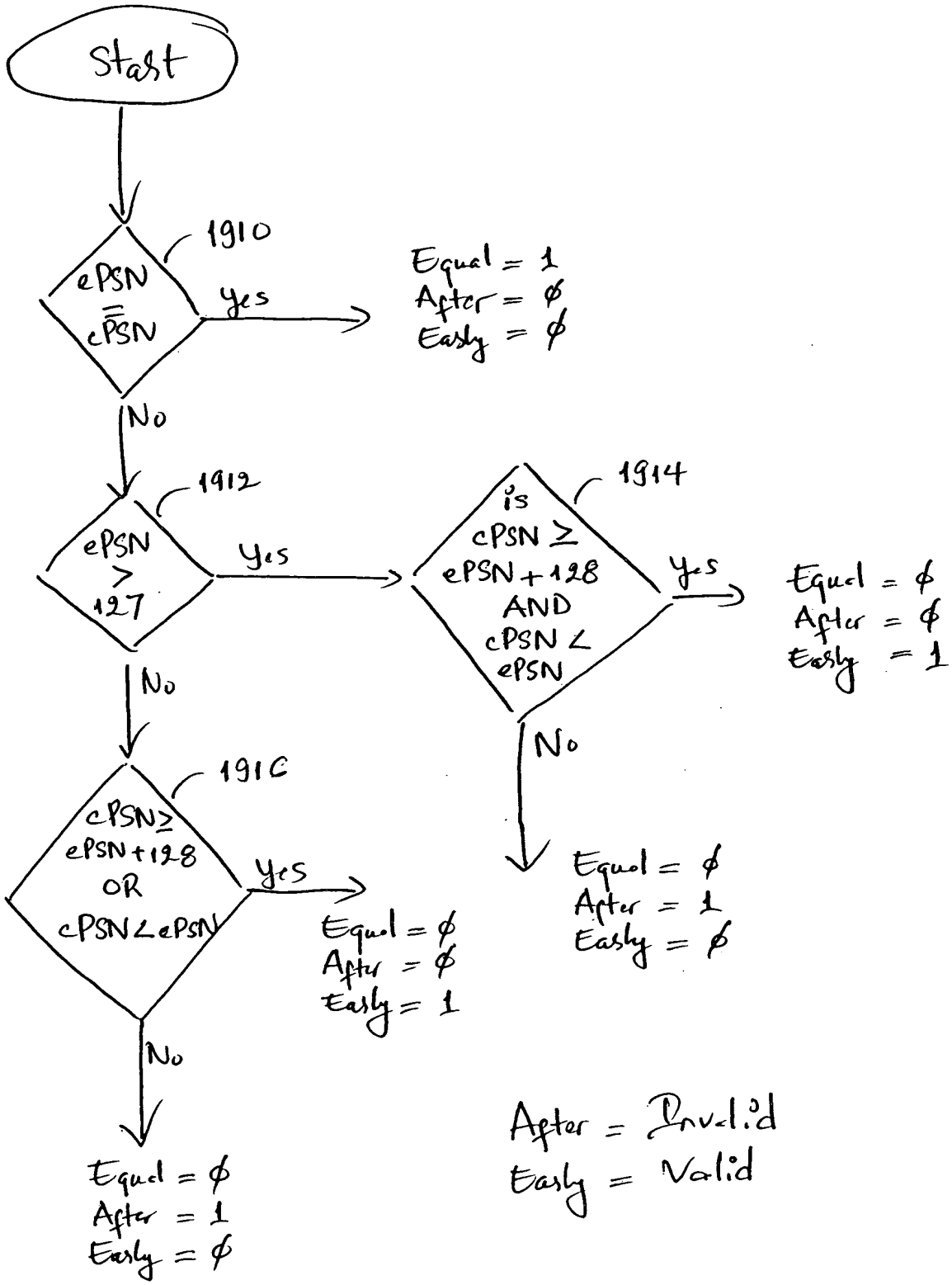

Start
1910
ePSN = cPSN
Yes
Equal = 1
After = ϕ
Early = ϕ
No
1912
ePSN > 127
Yes
1914
is cPSN ≥ ePSN+128 AND cPSN < ePSN
Yes
Equal = ϕ
After = ϕ
Early = 1
No
Equal = ϕ
After = 1
Early = ϕ
No
191C
cPSN ≥ ePSN+128 OR cPSN < ePSN
Yes
Equal = ϕ
After = ϕ
Early = 1
No
Equal = ϕ
After = 1
Early = ϕ
After = Invalid
Early = Valid

FIG. 20

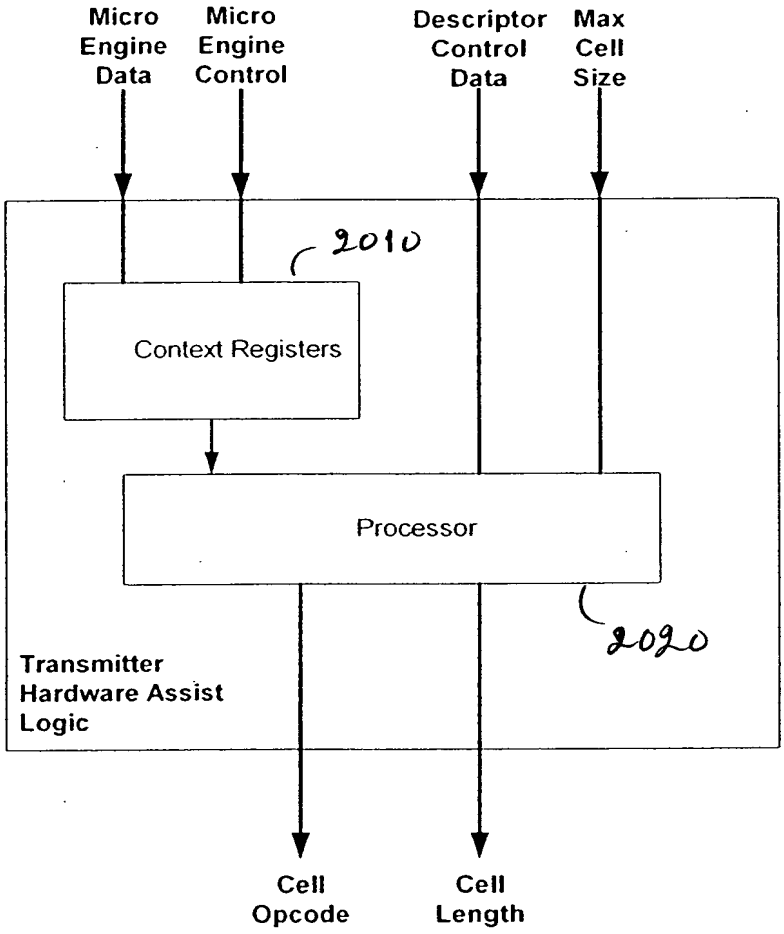

Micro Engine Data
Micro Engine Control
Descriptor Control Data
Max Cell Size
2010
Context Registers
Processor
2020
Transmitter Hardware Assist Logic
Cell Opcode
Cell Length

FIG. 21

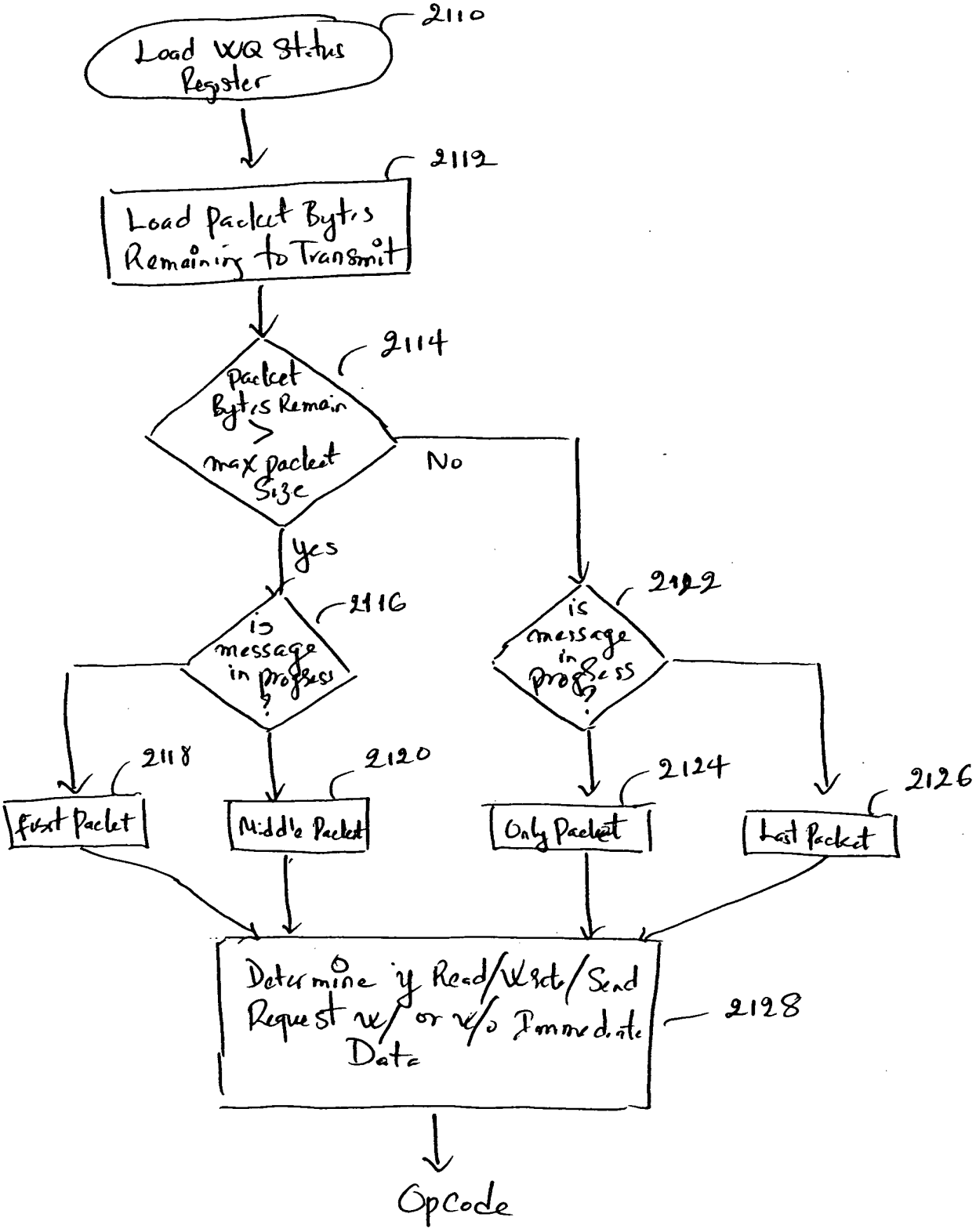
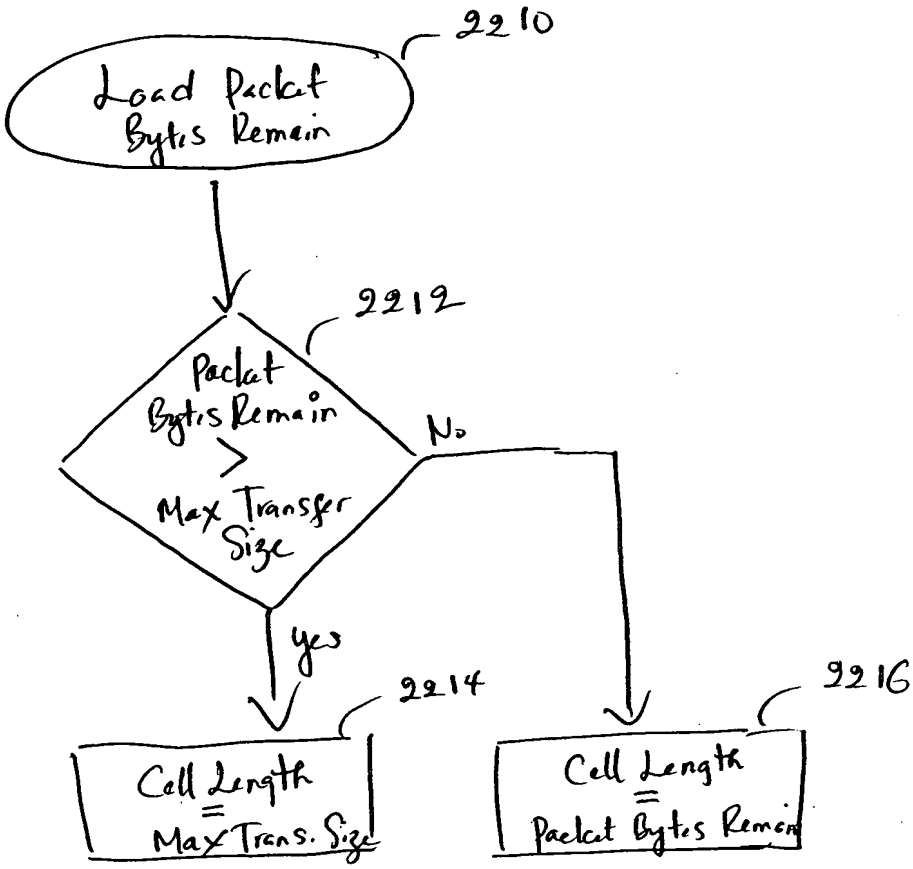

2110
Load WQ Status Register
2112
Load Packet Bytes Remaining to Transmit
2114
Packet Bytes Remain > max packet Size
No
Yes
2116
is message in progress?
2122
is message in progress?
2118
first Packet
2120
Middle Packet
2124
Only Packet
2126
Last Packet
Determine if Read/Write/Send Request w/ or w/o Immediate Data
2128
Opcode

FIG. 22


2210
Load Packet Bytes Remain
2212
Packet Bytes Remain > Max Transfer Size
No
Yes
2214
Cell Length = Max Trans. Size
2216
Cell Length = Packet Bytes Remain